WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a memory cell array having a plurality of memory cells arranged in rows and columns;

a counting circuit configured to receive a clock signal and counting a number of clock cycles of the clock signal;

a control circuit configured to receive an external control signal, and to generate an internal control signal on the basis of the external control signal and/or an output signal from the counting circuit;

a specification circuit configured to receive address signals in response to the internal control signal generated from the control circuit, and to designate a memory cell in said memory cell array;

a selection circuit configured to receive the address signals in response to the internal control signal from said control circuit, and to select one of a normal operation mode and a synchronous mode in a mode setting cycle; and

a data I/O circuit configured to input data into the memory cell selected by said specification circuit and to output the data from the memory cell selected by said specification circuit,

wherein in the normal mode, setting of address signals of the memory cell in said memory cell array by the specification circuit is effected irrespective of the clock signal, and in the synchronous mode, a

rising edge or a falling edge of the clock signal determines a setting timing of the address signals of the memory cell in said memory cell array by the specification circuit.

2. The semiconductor device according to claim 1, wherein the memory cell is one of a dynamic memory cell, a static memory cell and a non-volatile memory cell.

3. The semiconductor device according to claim 1, wherein the output of data begins a number of clock cycles (latency N) of the clock signal (latency N being a positive integer ≥ 2) after setting of the synchronous mode, a different one of the data being output at each of the clock cycles after the output begins until the plurality of data is output.

4. The semiconductor device according to claim 3, wherein the latency N is determined by externally supplying a latency control signal.

5. The semiconductor device according to claim 3, wherein the latency N is variably programmed.

6. The semiconductor device according to claim 1, wherein the address signals include row address signals and column address signals; and

the external control signal includes a row enable signal for inputting row address signals into the specification circuit and a column enable signal for, after a row address is determined in the specification circuit by

an input of the row address signals, inputting the column address signals into the specification circuit.

7. The semiconductor device according to claim 1, wherein the address signals include at least row address signals, and

the external control signal includes at least a row enable signal for inputting row address signals into the specification section.

8. The semiconductor device according to claim 1, wherein the address signals include at least column address signals, and

the external control signal includes at least a column enable signal for inputting column address signals into the specification circuit.

9. The semiconductor device according to claim 1, wherein the counting circuit includes a series of shift registers for transferring a trigger signal in response to a signal synchronized with the clock signal.

10. The semiconductor memory device according to claim 9, wherein each of the shift registers includes clocked inverters which operate in response to the signal synchronized with the clock signal.